Corres. and Mail
BOX AF

AF/2880

Docket No.: 49657-844

PATENT

#10
Req. for Reconsid. of Petition 12/13/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	: **RESPONSE UNDER 37 CFR 1.116**
	: **EXPEDITED PROCEDURE**
Akira OHTA, et al.	:
	:
Serial No.: 09/717,215	: Group Art Unit: 2817
	:
Filed: November 22, 2000	: Examiner: Joseph Chang
	:

For: HIGH EFFICIENCY AMPLIFIER WITH AMPLIFIER ELEMENT, RADIO TRANSMISSION DEVICE THEREWITH AND MEASURING DEVICE THEREFOR

REQUEST FOR RECONSIDERATION

Box AF
Commissioner for Patents
Washington, DC 20231

Sir:

This Request is submitted in response to the Office Action mailed September 5, 2002.

Claims 1-6, 8, 33-38, and 40 presented for examination stand rejected under 35 U.S.C. 102(b) as being anticipated by Makino et al. 5,945,887. This rejection is respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the Examiner. ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Thorpe***, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); ***In re Piasecki***, 745 F.2d 1468, 223

USPQ 785 (Fed. Cir. 1984). To satisfy this burden, therefore, each and every element of the claimed invention must be shown by the Examiner to be disclosed in Makino.

Claim 1 recites a high efficiency amplifier, connected to a non-reciprocal circuit element having an input impedance lower than a standard impedance and an output impedance substantially equal to said standard impedance. The amplifier comprises:

-an input terminal to receive an input signal;

-an output terminal connected to said non-reciprocal circuit element;

-an amplifier element to amplify said input signal; and

-one or a plurality of harmonic processing circuits arranged between said amplifier element and said output terminal to process a harmonic in an output signal of said amplifier element.

Independent claim 33, among other elements, also recites a high efficiency amplifier including:

-an input terminal to receive an input signal,

-an output terminal connected to the non-reciprocal circuit element via the transmission line,

-an amplifier element to amplify the input signal, and

-one or a plurality of harmonic processing circuits arranged between the amplifier element and the output terminal to process a harmonic in an output signal of the amplifier element.

The Office Action contains a statement that "Examiner pointed out the harmonic processing circuit as being 6 or 16 in figure 2, which is between the amplifier 13 and the output terminal (50ohms terminal)." (page 2, lines 13-15).

Considering the Makino reference, FIG. 2 shows an amplifier 10 coupled to an isolator 1. The amplifier 10 includes "an output matching circuit 16, the output of which is connected to isolator 1." (col. 4, lines 41-43). "In isolator 1 of the present embodiment, an impedance conversion circuit 6 is added to port P1." (col. 4, lines 46-47).

Accordingly, the impedance conversion circuit 6 is provided in the isolator 1, rather than between the amplifier element and the output terminal of the amplifier, as claims 1 and 33 require.

The Applicants' representative discussed this issue during a telephone conference with Examiner Joseph Chang, whose assistance in prosecuting the present application is greatly appreciated. The Examiner indicated that he considered the 50-ohm output of the isolator 1 to be the claimed output terminal. However, as the Applicants' representative pointed out, claims 1 and 33 specifically recite that the claimed output terminal is an element of the high efficiency amplifier connected to a non-reciprocal circuit element.

As the impedance conversion circuit 6 is not arranged between the amplifier element and the output terminal of the amplifier 10, this circuit cannot be considered to correspond to the claimed harmonic processing circuit.

Moreover, as pointed out in the Applicants' previous response, the output matching circuit 16 also cannot be considered to correspond to the claimed harmonic processing circuit. In particular, Makino teaches that the output matching circuit 16 having output impedance of 2 to 12.5 ohms removes the reactance component only. As one skilled in the art would realize, the reactance component is eliminated for fundamental wave matching. Thus, the output matching circuit 16 does not need to process harmonics to carry out its output matching functions.

It is noted that the reference does not disclose that the output matching circuit 16 is a harmonic processing circuit, or a circuit for processing harmonics. It appears that the Examiner believes that the output matching circuit inherently processes harmonics.

However, to establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

As demonstrated above, the output matching circuit 16 does not need to process harmonics to carry out its output matching functions. Accordingly, the reference provides no reason to conclude that the output matching circuit 16 necessarily process harmonics.

Hence, the reference neither expressly nor under principles of inherency, describes the claimed harmonic processing circuit recited in claims 1 and 33.

Dependent claims 2-6, 8, 34-38, and 40 are defined over the reference at least for the reasons presented above in connection with independent claims 1 and 33. Moreover, the Examiner did not address limitations of the dependent claims. However, it is respectfully submitted that the reference does not teach or suggest, for example, limitations of claims 3-6, and 35-38.

Applicants, therefore, respectfully submit that the rejection of claims 1-3 and 8-10 under 35 U.S.C. § 102 as anticipated by Makino et al. is untenable and should be withdrawn.

In addition, Applicants submit that the claimed invention would not be obvious over the prior art. In particular, as described on page 3, line 26 to page 4, line 4 of the specification, the problem solved by the claimed invention relates to reducing the harmonic-related leakage power,

which increases when the output of the amplifier is connected to the impedance of 50 Ohms or less (see for example, the prior art structure shown in FIG. 36 of the present application).

The claimed harmonic processing circuits are provided to reduce this harmonic-related leakage power. To efficiently perform their functions, the harmonic processing circuits should be provided in the amplifier, i.e. as close as possible to the transistor, which is an amplifying element in the amplifier. Such an arrangement allows the harmonic processing circuits to increase the reflectance of the harmonics for that transistor. The increased reflectance of the harmonics makes it possible to achieve the harmonic processing corresponding to processing by the class F amplifier or inverse class F amplifier. As a result, the efficiency of the processing is substantially improved.

It is noted that Makino expressly teaches away from the claimed invention because the reference suggests providing the impedance conversion circuit 6. Similar structure having the fundamental wave matching circuit 112 corresponding to the impedance conversion circuit is shown in the prior art FIG. 35 of the present application. Typically, the impedance conversion circuit functions as a low-pass filter. Accordingly, there is no loss generated in the circuitry corresponding to the output matching circuit 108 in FIG. 35. Hence, the structure with the impedance conversion circuit does not need the claimed harmonics processing circuit to reduce the harmonic-related leakage power.

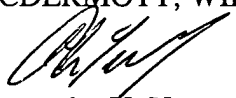
Therefore, the claimed invention is not obvious over the prior art.

In view of the foregoing, and in summary, claims 1-6, 8, 33-38, and 40 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 AVY:MWE
Facsimile: (202)756-8087
Date: December 2, 2002